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Surface Selectively Deposited Organic Single-crystal Transistor Arrays with High Device Performance

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A method for patterning organic single-crystal transistor arrays via surface selective deposition is presented. Solvent-vapor annealing is applied for the formation of organic crystals under ambient conditions. The devices are fabricated with a dual-gate structure, which allows the investigation of device performances of bottom-gate/top-contact (BG/TC) and top-gate/top-contact (TG/TC) structures based on the same crystals. The resulting BG/TC devices exhibit the field-effect mobility (μ_{FET}) up to 3.5 cm^2/Vs. And μ_{FET} is influenced by the contact resistance, resulting in large variation in device performance. On the other hand, TG/TC structure exhibits better performance with smaller variation. The highest μ_{FET} is 7.4 cm^2/Vs.

Keywords Surface selectively deposition; organic single crystals; organic field-effect transistor; solvent-vapor annealing

Introduction

In recent years, organic single crystals (OSCs) have attracted tremendous interest, since they are ideal materials for the application of organic field-effect transistors (OFETs) with the highest device performance [1–3]. The excluding of grain boundaries and molecular disorders, which frequently act as scattering sites, is the principle advantage of OSCs [4]. For their potential application in real products, patterning of OSC transistor arrays is one of the common considerations [5]. Various techniques have been well developed [5–10], among which surface selective deposition by using self-assembly molecules (SAMs) is one of the promising methods [8–10]. However, for the patterned OSC transistor arrays, the improvement of the device performance with small variation is still a great challenge.

Here, we propose a fabrication process for the OSC transistor arrays via surface selective deposition and solvent-vapor annealing [11]. P-type organic semiconducting material of dioctylbenzothienobenzothiophene (C8-BTBT) is spin-coated from a mixture solution with polymer dielectric of polymethylmethacrylate (PMMA). And solvent-vapor annealing is applied for the formation of C8-BTBT OSCs. The transistors are fabricated with a

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dual-gate architecture. Thus, it is allowed to investigate the device performances of bottom-gate/top-contact (BG/TC) and top-gate/top-contact (TG/TC) structures based on the same organic crystals. The resulting devices with BG/TC structure exhibit good electrical performance. However, variation in performance has been observed, which is due to the contact effect at the metal/semiconductor interfaces. On the other hand, higher performance and smaller variation is obtained in TG/TC transistors. And it is due to that the performance of TG/TC devices has less dependence on the access resistance.

Experimental

C8-BTBT and PMMA are used as the organic semiconductor and polymer dielectric, respectively. The fabrication process of dual-gate transistors is shown in Fig. 1(a). For

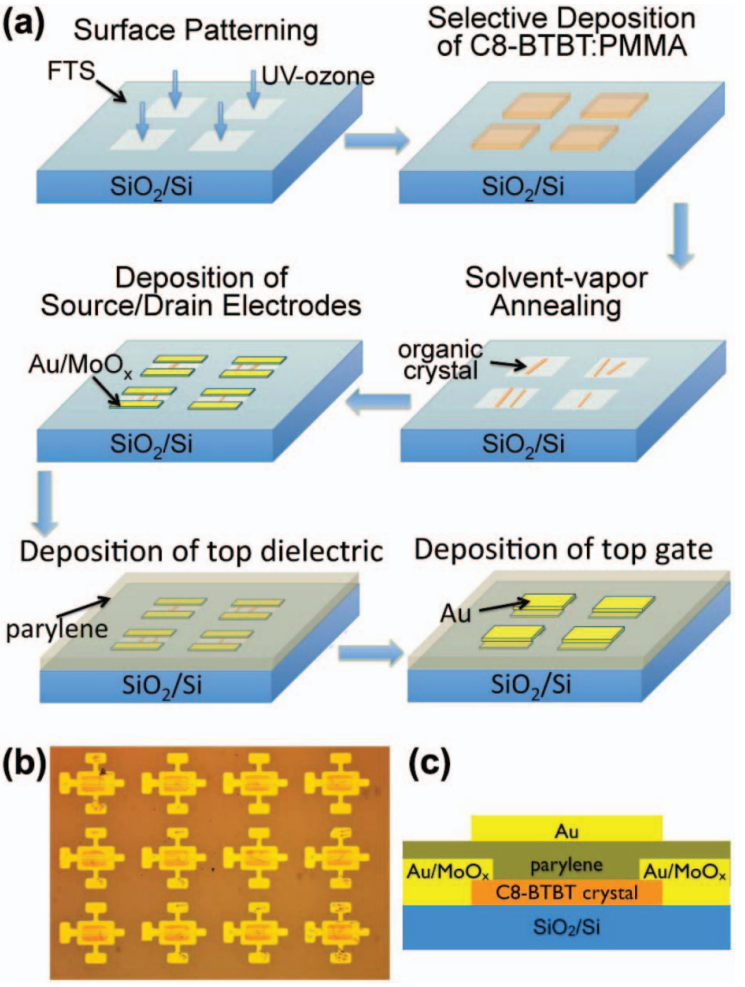

Figure 1. (a) Fabrication process of the organic field-effect transistor arrays based on dioctylbenzothienobenzothiophene (C8-BTBT) single crystals by using surface selective deposition. (b) The fabricated transistor arrays with dual-gate architecture. (c) Schematic of the dual-gate structure.

the patterning of substrate surface wettability, self-assembly molecule of (tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane (FTS) is applied. First, a mixture solution of C8-BTBT (0.5 wt%) and PMMA (1 wt%) in anisole is spin-coated on the pre-cleaned SiO_2 (200 nm)/Si substrate, whose surface wettability has been patterned by using UV-ozone treatment with a shadow mask after FTS deposition. A double layer is formed due to the phase separation, resulting in a 20 nm thick PMMA underneath the C8-BTBT layer. The as-spun film with polycrystalline C8-BTBT is then annealed with chloroform saturated vapor under ambient conditions at room temperature and reorganizes into single crystals via self-assembly. And then, MoO_X and Au are thermally evaporated subsequently through shadow mask to form the source and drain electrodes. For TG/TC structure, 580 nm parylene as the top dielectric is deposited by physical vapor transport. And then a 50 nm thick Au is thermally evaporated onto the substrate to form the top gate. The electrical performance of FET arrays is measured under vacuum using an Agilent 4156C semiconductor parameter analyzer.

Results and Discussion

The polymer, PMMA, is critical for the formation of C8-BTBT crystals, providing a high molecular mobility to facilitate the rearrangement of C8-BTBT molecules over a large distance on the substrate [11]. Figures 1(b) and (c) present the OSC transistor arrays after the deposition of top gate and the schematic of the dual-gate structure, respectively. Figure 2(a) shows a typical individual BG/TC transistor on the substrate based on C8-BTBT OSCs. The organic crystals are well confined in the patterned region after the solvent vapor annealing. And the crystals exhibit strong birefringence under the cross-polarized microscope, confirming their crystalline nature (Fig. 2(b)). Moreover, there are only several crystals in the channel regions after the solvent-vapor annealing. Therefore, we calculate the channel width and length from the sizes of each crystal.

Figure 3(a) shows the typical transfer characteristics of the BG/TC transistors based on the C8-BTBT single crystals as shown in Fig. 2(a). The figures show negligible hysteresis. The field-effect mobility (μ_{FET}) in the saturated region is calculated using the equation:

$$I_D = \mu_{\mathrm{FET}} C_i (W/2L)(V_G - V_T)^2, \tag{1}$$

where W and L are the width and length of the crystal, respectively, and C_i is the capacitance per unit area of the gate dielectrics, V_T is the threshold voltage. The C_i is 1.5×10^{-8} F/cm^2

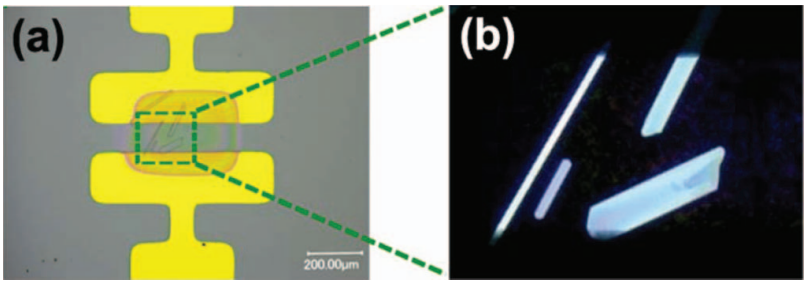

Figure 2. (a) shows the typical individual device on the substrate before the deposition of top dielectric. (b) shows strong birefringence of the crystals in the green square in (a) under the cross-polarized microscope, confirming their crystalline nature.

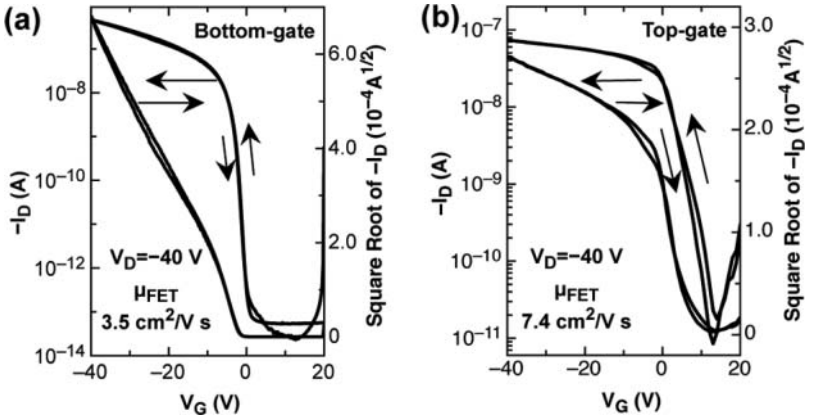

Figure 3. Typical transfer curves of (a) bottom-gate/top-contact and (b) top-gate/top-contact devices based on the crystal as shown in Figs. 2(a) and 2(b).

with the consideration of double-layered gate dielectrics of PMMA/SiO_2. The on/off ratio exhibited in the transfer curve is greater than 10^7, and the threshold voltage (V_T) and subthreshold swing (S) are −0.6 V and 0.7 V/dec, respectively. Taking the slope of the curvature, μ_{FET} is estimated as high as 3.5 cm^2/Vs.

Although the devices show promising electrical performance, we observe variation in μ_{FET} ranging from 0.4 to 3.5 cm^2/Vs. The average value of μ_{FET} (μ_{ave}) is calculated out of seven devices to be 1.5 cm^2/Vs. with a standard deviation (σ) of 0.9 cm^2/Vs. Such variation is frequently caused by the contact effect at the metal/semiconductor interfaces [6,12], which has also been discussed in our previous work [8].

Based on the notion that the contact resistance can be influenced by the crystal thickness, it is expected that the TG/TC devices can give better electrical performance and smaller variation. Figure 3(b) shows the transfer characteristics of the top-gate device based on the same C8-BTBT crystals as shown in Fig. 2(a). Different device behavior is observed, exhibiting that V_T is shifted to a positive value of 6.3 V. And the calculated μ_{FET} reaches to 7.4 cm^2/Vs, which is higher than that in the BG/TC structure. Besides, all the measured seven samples have higher μ_{FET} in the TG/TC structure than that obtained from BG/TC devices. The calculated μ_{ave} of the TG/TC devices is as high as 5.0 cm^2/Vs. with a standard deviation (σ) of 2.3 cm^2/Vs. Thus, the values of σ/μ_{ave} are 0.60 and 0.46 for the BG/TC and TG/TC devices, respectively. The higher device performance and smaller variation in the TG/TC transistor arrays can be due to that the conducting channel is close to the interface of crystals and top dielectric, resulting in less dependence of the performance on the access resistance.

Conclusion

In conclusion, we fabricated organic single-crystal transistor arrays by applying surface selectively deposition. C8-BTBT single-crystals are formed via solvent-vapor annealing. The transistor arrays with the BG/TC structure exhibit μ_{FET} up to 3.5 cm^2/Vs. However, variation in μ_{FET} is also observed, which is caused by the contact resistance. Furthermore, the TG/TC transistor arrays show higher device performance and smaller variation. And the highest μ_{FET} obtained is 7.4 cm^2/Vs. Although the highest value of mobility in the current

work is lower than the best in our previous work [11], the comparison of device performance based on the same crystals from the TG/TC and BG/TC structures is presented, indicating the dependence of electrical performance on device structure.

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